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(54) Title: RISC MICROPROCESSOR ARCHITECTURE

(57) Abstract

The microprocessor (100) executes at 100 native MIPS peak performance with a 100-MHz internal clock frequency. The CPU instruction sets are hardwired, allowing most instructions to execute in a single cycle. A "flow-through" design allows the next instruction to start before the prior instruction completes, thus increasing performance. MPU (108) contains 52 general-purpose registers, including 16 global data registers (104), an index register (132), a count register (134), a 16-deep addressable register/return stack (124), and an 18-deep operand stack (122). Both stacks contain an index register (128, or 130) in the top elements, are cached on chip, and, when required, automatically spill to and refill from external memory. The stacks minimize the data movement and also minimize memory access during procedure calls, parameter passing, and variable assignments. Additionally, the MPU contains a mode/status register (136) and 41 locally addressed registers (102) for I/O, control, configuration, and status. The CPU (100) contains both a high-performance, zero-operand, dual-stack architecture microprocessing unit (MPU) (108), and an input-output processor (IOP) (110) that executes instructions to transfer data, count events, measure time, and perform other timing-dependent functions. A zero-operand (stack) architecture eliminates operand bits. Stacks also minimize register saves and loads within and across procedures, thus allowing shorter instruction sequences and faster-running code. Instructions are simple to decode and execute, allowing the MPU (108) and IOP (110) to issue and complete instructions in a single clock cycle - each at 100 native MIPS peak execution. Using 8-bit opcodes, the CPU (100) obtains up to four instructions from memory each time an instruction fetch or pre-fetch is performed. These instructions can be repeated without rereading them from memory. This maintains high performance when connected directly to DRAM, without a cache.

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